

Form PTO-1449

1 of 3

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

DEC 22 2003

(Use separate sheets if necessary)

Docket Number (Optional)

TSMC-01-037 B

Application Number

10/682,052

Applicant

Kou-Reg Peng et al.

Filing Date

10/09/03

Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED DATE IF APPROPRIATE
J	6118155	9/12/00	Voldman	257	360	6/16/99
	5674761	10/7/97	Chang et al.	437	29	5/2/96
	5856214	1/5/99	Yu	438	133	3/4/96
	6096584	8/1/00	Ellis-Monaghan et al.	438	151	3/12/98
	4616404	10/14/86	Wang et al.	29	576 B	4/30/84
	6229157	5/8/01	Sandhu	257	75	8/11/99
	6232163	5/15/01	Voldman et al.	438	212	7/28/99
J	6015993	1/18/00	Voldman et al.	257	355	8/31/98

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- The paper "On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Technology for Smart Card Application," by Wang et al., EOS/ESD Symposium 00-266, pp. 3A.4.1 - 3A.4.10.
- "On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Process," Ker et al., IEEE Journal of Solid-State Circuits, IEEE, New York, Vol. 36, No. 4, April 2001, pp. 678-686.

EXAMINER

DATE CONSIDERED

4/06

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

		OTHER DOCUMENTS (including Reports, Notes, Letters, and other documents)
		"Design of the Turn-On Efficient Power-Rail ESD Clamp Circuit with Stacked Polysilicon Diodes," Ker and Chen, Proceeding of the 2001 Int'l Symp. on Circuits and Systems, IEEE, New York, 2001, pp. IV-758-IV-761
		

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